ABSTRACT:

Computer architectures consist of a fixed data path, which is controlled by a set of control words. Each control word controls part of the data path. Each set of instructions generates a new set of control words. In case of a VLIW processor, multiple instructions are packaged into one so-called VLIW instruction. A VLIW processor uses multiple, independent functional units to execute these multiple instructions in parallel. Application specific domain tuning of a VLIW processor requires that instructions having varying requirements with respect to the number of instruction bits they require can be encoded in a single VLIW instruction, such that an efficient encoding and encoding of instructions is maintained. The present invention describes a processing apparatus as well as a processing method for processing data, allowing the use of such an asymmetric instruction set. The processing apparatus comprises at least a first (UC_0) and a second issue slot (UC_3), wherein each issue slot comprises a plurality of functional units ($FU_{01} - FU_{02}$, $FU_{30} - FU_{32}$). The first issue slot (UC_0) is being controlled by a first control word (411) being generated from a first instruction (InstrA) and the second issue slot is being controlled by a second control word (417) being generated from the second instruction (InstrD), the width of the first control word (411) being different from the width of the second control word (417). By varying the width of a corresponding control word, instructions requiring a different number of bits can be efficiently encoded in a VLIW instruction while allowing an efficient instruction decoding as well.

Fig. 3